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LSI/VLSI ION IMPLANTED GaAs IC PROCESSING

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Microelectronics Research and Development Center
Thousand Oaks, CA. 91360

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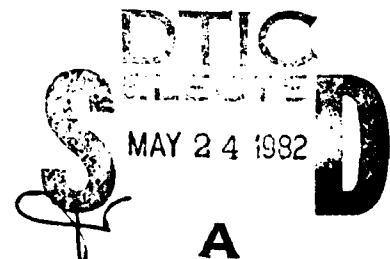R. Zucca
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This report covers the fourth quarter of a program aimed at fully realizing the potential of GaAs for digital integrated circuits employing depletion mode MESFETs. During this reporting period, studies of the factors affecting the reproducibility of the FET channel implants have continued. It appears that material related variations, which used to be dominant, have decreased with LEC material, and are now on the order of process related variations. Research at Caltech has continued in the area of low temperature

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annealing of GaAs. Although the lattice can apparently be reordered to a near virgin state, according to the backscattering data, electrical measurements reveal very little electrical activity of the implanted dopant. Test structures for measuring the width of second level metal lines, and for monitoring the yield of very long parallel second level metal lines have been used. A magnetron sputtering technique for deposition of second level metallization is resulting in higher yield of long parallel lines. Reliability of GaAs integrated circuits was being studied using accelerated life test. Measurements on ring oscillators aged under bias at 296°C and 320°C showed median lifetimes before 20% deterioration of oscillation frequency of 14 and 46 hours, respectively. Lifetimes of ~10^{13} hours at room temperature are estimated from these data. Work on MESFET device modeling during this period was concentrated on: a) modeling FETs with an ion implanted profile, as opposed to uniformly doped FETs, b) developing techniques for calculating the small-signal parameters of the FETs.

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FOREWORD

The research covered in this report is carried out in a team effort having the Rockwell International Microelectronics Research and Development Center as the prime contractor, with two universities and a crystal manufacturer as subcontractors. The effort is sponsored by the Defense Sciences Office of the Defense Advanced Research Projects Agency. The contract is monitored by the Air Force Office of Scientific Research. The Rockwell program manager is Fred H. Eisen. The principal investigators for each organization are:

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Crystal Specialties	J. Burns

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TECHNICAL SUMMARY

This report covers the fourth quarter of a program on LSI/VLSI ion implanted planar GaAs integrated circuit processing. The goal of this program is to realize the full potential of GaAs digital integrated circuits employing depletion mode MESFETs by developing the necessary processing methods and material capabilities to extend device complexity to VLSI. In the fourth quarter fabrication of the first wafers with mask set AR6, the last mask set to be employed with one inch wafers, was completed. Work on circuit reliability has continued, while process steps that may be limiting circuit yield are being investigated. The subcontractors' work continues to show progress.

Substrate Material and Ion Implantation

Studies of the factors affecting the reproducibility of the FET channel implants have continued. Experiments to discriminate between material dependent and process induced variations of depletion voltage from run to run were carried out. Preliminary results are discussed. It appears that material related variations, which used to be dominant, have decreased with LEC material, and are now on the order of process related variations.

Research at Caltech has continued in the area of low temperature annealing of GaAs. Previous work revealed that a high degree of crystalline order could be restored after the formation of a thin amorphous layer by ion implantation, by annealing at low temperatures (400°C). In the recent studies, Te was implanted and both electrical and backscattering measurements were performed. Although the lattice can apparently be reordered to a near virgin state, according to the backscattering data, electrical measurements reveal very little electrical activity of the implanted dopant.

Circuit Fabrication and Process Stabilization

Processing on mask set AR6 containing a SD^{2}FL 8 × 8 multiplier was begun in the quarter; at the end of the quarter, the first lot of wafers was completed, and several lots of wafers were being fabricated.

Test structures for measuring the width of second level metal lines, and for monitoring the yield of very long parallel second level metal lines have been used. A magnetron sputtering technique for deposition of second level metallization is resulting in higher yield of long parallel lines.

Reliability of GaAs integrated circuits was being studied using accelerated life test. Measurements on ring oscillators aged under bias at 296°C and 320°C showed median lifetimes before 20% deterioration of oscillation frequency of 14 and 46 hours, respectively. Lifetimes of $\sim 10^{13}$ hours at room temperature are estimated from these data.

MESFET Device Modeling

Work during this period was concentrated on: a) modeling FETs with an ion implanted profile, as opposed to uniformly doped FETs, b) developing techniques for calculating the small-signal parameters of the FETs. Two analytical MESFET models were also under development.

1.0 INTRODUCTION

This report covers the fourth quarter of a program on LSI/VLSI Ion Implanted Planar GaAs IC Processing. The main objective of this program is to realize the full potential of GaAs digital integrated circuits by expanding and improving fabrication techniques as well as material growth, preparation and selection. The principal goal is to improve material and processing capabilities so that large wafers (over 2 inch diameter) can be processed in order to satisfy anticipated needs for high-speed low-power GaAs digital VLSI integrated circuits. In parallel with increasing circuit complexity and wafer size, the program is also directed toward the investigation of circuit reliability, and the development of processing techniques and circuit designs capable of attaining the highest reliability. Circuit design advancements are also explored with the introduction and implementation of multilevel logic circuits. Three subcontractors, the California Institute of Technology, North Carolina State University, and Crystal Specialties, Inc. are contributing to the program with their expertise in ion beam techniques, device modeling, and crystal growth, respectively.

While equipment preparation for processing of large wafer continues, several aspects of process development have received attention. The work in this area is aimed at improving device performance, process yield, and circuit reliability, and it is supported by a sustained effort in semi-insulating substrate analysis and ion implantation development. As a result of these combined activities, improvements in reproducibility of FET threshold voltage have been observed.

Reliability data have shown improved results in terms of operation at elevated temperature and time without failure. Ring oscillator thermal aging tests have yielded an estimate of 10^{13} hours time before failure at room temperature operation. Improvements in the second layer metallization process are being made with the utilization of a magnetron sputtering system for metal deposition. Higher yield is expected from this process step, which is also compatible with up to 3 inch wafer diameter. Processing wafers with mask set AR6 was under way during the fourth quarter, and the first lots of wafer was completed.

The research team at the California Institute of Technology has carried out some studies on low temperature annealing of GaAs. The team at North Carolina State University is continuing with a project on modeling of the low threshold GaAs MESFET usd in the SDFL circuits. This modeling activity is organized in three tasks: two dimensional modeling; Monte Carlo analysis; and an analytical model.

2.0 SEMI-INSULATING SUBSTRATE MATERIAL AND ION IMPLANTATION

Studies of the factors affecting the reproducibility of the FET channel implants have continued. Recent results are discussed in Section 2.1. Conclusions from the study of low temperature annealing of GaAs carried out at Caltech are discussed in Section 2.2.

2.1   Reproducibility of Low Dose Implantations in Semi-Insulating GaAs

The investigation of factors which influence the reproducibility of ion implanted layers has continued this quarter with particular attention given to the n^- Se implant used for the FET channel regions. A long-standing problem has been the difficulty of distinguishing implant variations that are due to process differences, from implant variations due to differences between substrate material properties. Data have been recently accumulated to separate the individual contributions of these two effects.

In order to observe the magnitude of the process-related variations alone, a test chip from a fixed control ingot was included in each of 47 different implant runs carried out over a period of 9 months. The test chips were processed in a nominally identical way (with, for example, nominally identical Si_3N_4 encapsulant thickness and implant dose). Measurements of the depletion voltage V_d (voltage necessary to deplete the carrier density to 10^{16} cm^{-3}) yielded the results shown in Fig. 2.1-1. The standard deviation of V_d over this distribution was found to be 153 mV (after excluding 12% of the runs which yielded anomalously low activation, probably related to contamination effects).

Fig. 2.1-1
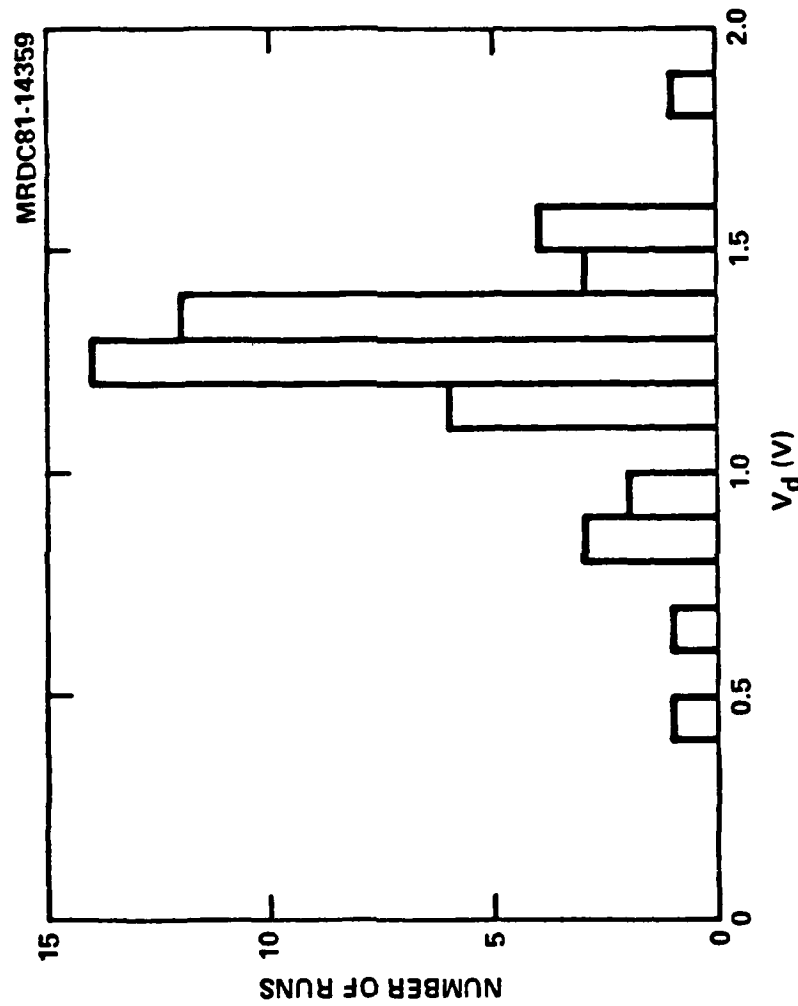
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NUMBER OF RUNS

V_d (V)

Fig. 2.1-1   Histogram of depletion voltages for a large number of tets chips from the same ingot, all processed in identical way over period of 9 months.

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In order to determine the variations in implant results that are re-
lated to substrate material alone, an experiment was conducted in which test
chips from a number of different ingots were processed simultaneously. Twelve
Bridgman ingots (obtained from Crystal Specialties and Mitsubishi-Monsanto) were
represented, as well as twelve LEC ingots (grown at Rockwell). The ingots were
preselected according to the standard qualification tests. The distribution of
depletion voltage V_d shown in Fig. 2.1-2 was obtained. For the Bridgman materi-
als the standard deviation of V_d was 304 mV (after excluding 2 of the wafers
with anomalously high V_d). The corresponding standard deviation was lower for
the LEC ingots, with a value of 170 mV. An even more favorable standard devia-
tion of V_d is observed if the population under test is restricted to those LEC
ingots grown after the first 10 runs of the crystal puller. All of the 8 re-
cently grown ingots in the test were nominally undoped and pulled from PBN
crucibles. The standard deviation of V_d observed for these 8 ingots was 81 mV.

The measured results indicate that substrate variations have histori-
cally been the largest contribution to implant variability, but with recently
available LEC material these variations appear to be significantly reduced. A
larger data base is needed to confirm the extent of the improvement. Process-
induced variations are now of comparable significance to the material-related
variations.

In order to place in perspective the magnitudes of the standard
deviations obtained in these experiments it is important to note that a special
procedure is employed at Rockwell to reduce run-to-run implant variations in the
fabrication of ICs. For each lot, a preliminary test is made. This test pro-
vides feedback concerning the behavior of the lot and based on this information,
the implant dose is adjusted in order to maintain a constant threshold voltage.
The sequence is illustrated in Fig. 2.1-3. A lot of wafers (consisting of
neighboring slices from the same ingot) is simultaneously processed through the
wafer cleaning step and Si_3N_4 encapsulation. Test chips from a representative
wafer of the ingot are also included in these steps. The test chips are then
implanted, annealed, and tested for depletion voltage. On the basis of the
results obtain , an appropriate implant fluence is determined for the wafers of
the lot. This feedback procedure reduces significantly the variations obtained

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Rockwell LEC
$\sigma_V = 170$ mV
(recent ingots 81 mV)

Bridgman
$\sigma_V = 304$ mV *

*16% excluded

V_d (V)
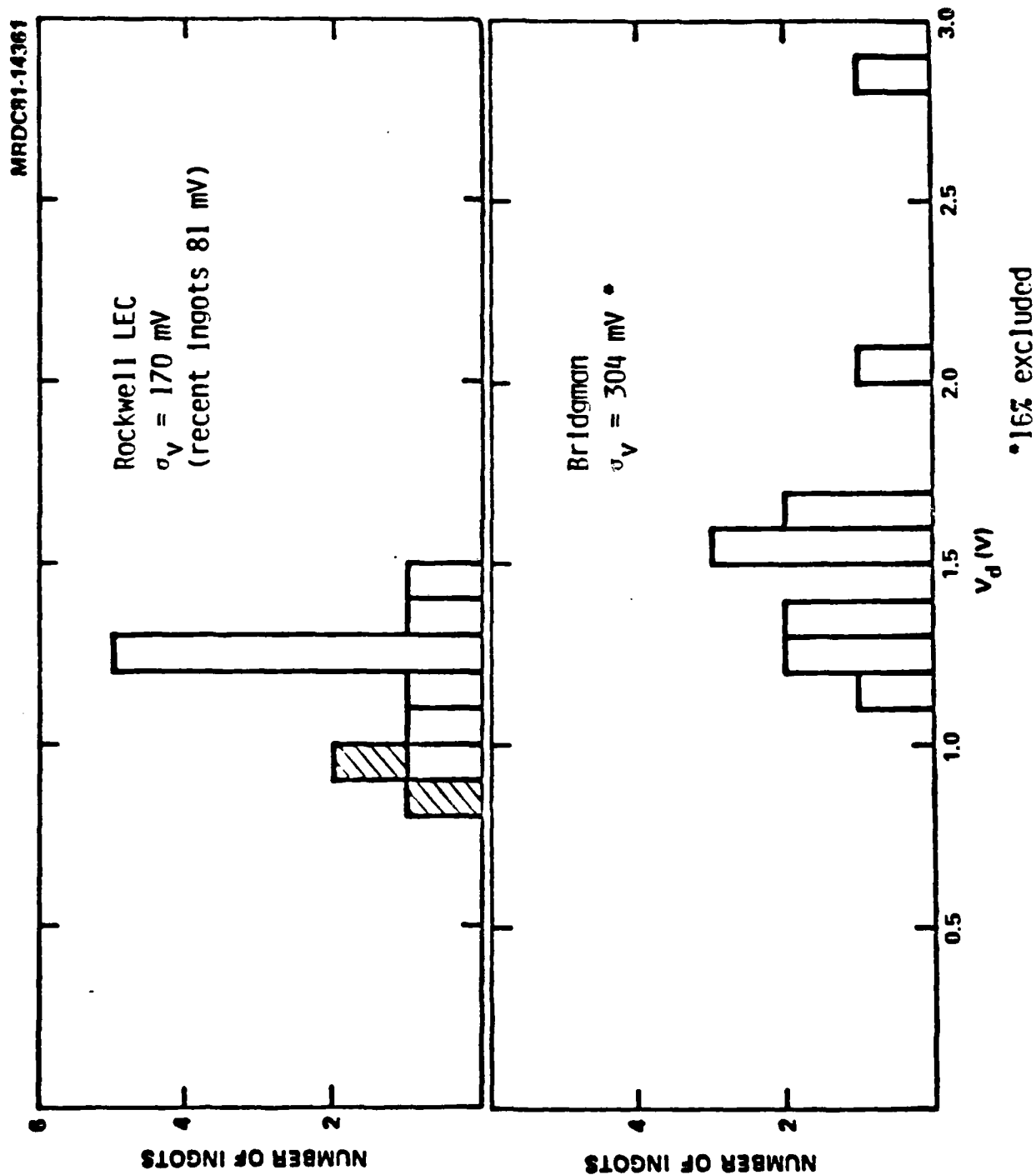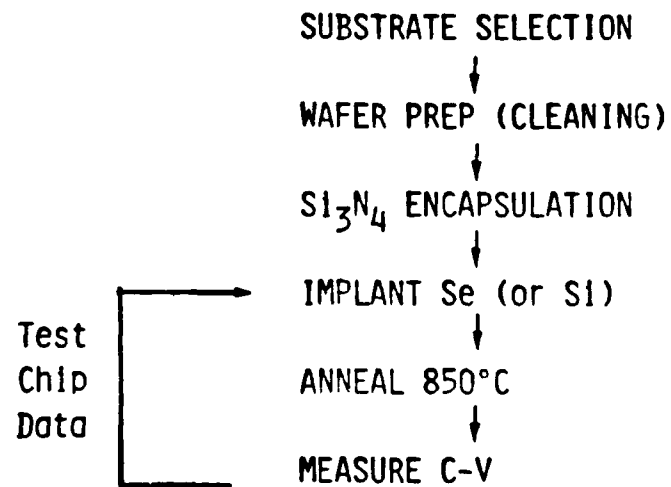
NUMBER OF INGOTS

NUMBER OF INGOTS

Fig. 2.1-2   Histograms of depletion voltages for a number of test chips from a Bridgman and LEC ingot, respectively. The test chips were all processed simultaneously.

SUBSTRATE SELECTION

↓

WAFER PREP (CLEANING)

↓

Si_3N_4 ENCAPSULATION

↓

IMPLANT Se (or Si)

↓

ANNEAL 850°C

↓

MEASURE C-V

Test
Chip
Data

$\sigma_V = 110$ mV

Total variation

With Feedback

Fig. 2.1-3   Implantation process sequence.

on an open loop basis. Accordingly, as reported in the previous quarter,[1] the run-to-run standard deviation of threshold voltage in IC wafers observed over a long period of time (6 months) has been 110 mV, which is lower than both the open loop contributions of the process-induced variations and substrate effects. This standard deviation is more than adequate for the high-yield fabrication of ICs based on SDFL logic.

The present understanding of the distinct contributions to the run-to-run standard deviation of threshold voltage V_p, is summarized in Fig. 2.1-4. The various process-induced contributions have been in most cases estimated on the basis of the measured sensitivity of V_p to a given parameter (for example, sensitivity of V_p to implant dose at 10^{-12} V/cm^{-2}) coupled with estimates of the control maintained over that parameter (for example, implant doses are believed maintained to $\pm$ 1%). To estimate the standard deviation σ_{net} resulting from all factors acting simultaneously, the rule

$$\sigma_{net} = \sqrt{\sum_i \sigma_i^2} \tag{1}$$

should be applied, since the factors are statistically independent. It may be seen that contamination effects are the dominant process-induced cause of variation. Studies are currently under way to improve understanding of these effects.

2.2 Low Temperature Annealing of GaAs

Room temperature implantation and low temperature ($\leq$ 60°C) regrowth have been subjects of investigation at Caltech and several other laboratories recently.[1-6] The main motivation for this work has been the hope of simplifying the process of electrical activation of ion implants into GaAs, and the wish to explore crystal regrowth properties in 3-5 compounds. In recent studies[1,2] it was shown that <100> GaAs that has been amorphized to a depth of $\leq$ 400Å by implantation can regrow at 400°C with a crystal quality that appears from spectra of channeled He backscattering to be almost as good as that of virgin material. More recently, the regrowth process for shallow implantations of dopant Te ions has been explored. Te was chosen 1) because it is a well known n-type dopant in

Standard Deviation σ

PROCESS-RELATED VARIATIONS   150 mV

    Implant dose   :   25 mV
    Implant energy   :   12 mV
    Si_3N_4 thickness   :   70 mV
    Anneal parameters   :   ~   10 mV
    Schottky barrier   :   ~   50 mV
    Deep electron traps   :   < 5 mV
    Contamination   :   120 mV

MATERIAL-RELATED VARIATIONS   Bridgman   300 mV
                                       LEC   < 170 mV

TOTAL VARIATION (Open loop)   ~ 350 mV

TOTAL VARIATION (Using feedback of   110 mV
             test chip data)

Fig. 2.1-4   Variations of threshold voltage for ion implanted FETs.

GaAs, and 2) because Te_2^+ molecules can readily be formed by ionization of Te vapor, facilitating low energy implantations. The question addressed was whether electrical activation could be achieved by low-temperature regrowth of shallow amorphized GaAs layers.

Semi-insulating <100> wafers of Cr-doped GaAs were implanted at room temperature with 80 keV Te_2^+ molecules to doses of 1×10^{14} and 2×10^{14} atoms cm^{-2}. According to the tabulations of Gibbons et al.,[7] 40 keV incident Te atoms should have a projected range in GaAs of 144 A, with a standard deviation of 63 A. Annealing was conducted at 400°C in flowing dry argon for 60 min. Since the regrowth rate of <100> GaAs at this temperature is known to be at least 130 A min^{-1},[1] it is expected that all possible regrowth must have bee completed in this time. Backscattering analysis was conducted with a 1.5 MeV incident He^+ beam channeled along the <100> direction. A glancing exit geometry (scattering angle = 98°) was used to increase the depth resolution.

The spectra from the sample implanted to a dose of 1×10^{14} cm^{-2} are shwon in Fig. 2.2-1a, together with a spectrum for a channeled incident beam from an unimplanted GaAs sample. It is evident that the implantation created an amorphous layer with a thickness of ~ 500 A. One can also see that the annealing resulted in good regrowth of this layer back to the sample surface. The spectrum for channeling incidence deviates only slightly from that obtained with virgin material, viz. a slightly larger surface peak caused by greater surface disorder and slightly greater dechanneling. Similar spectra are shwon for the implantation to a dose of 2×10^{14} cm^{-2} in Fig. 2.2-1b. Here the initial amorphous thickness is ~ 600 A, and again the backscattering spectrum with the channeled beam indicates excellent regrowth, the beam sensing only a low concentration of added defects. For both implantation doses, the abundance of Te atoms was too low for the Te signal in the backscattering spectra to be discerned in a statistically significant manner.

Sheet resistance measurements were performed on the samples by the van der Pauw method both before and after furnace annealing. The results are shown in Table 2.2-1. The values are high after implantation, but increase even further as a result of the annealing. Such an increase of resistance has been
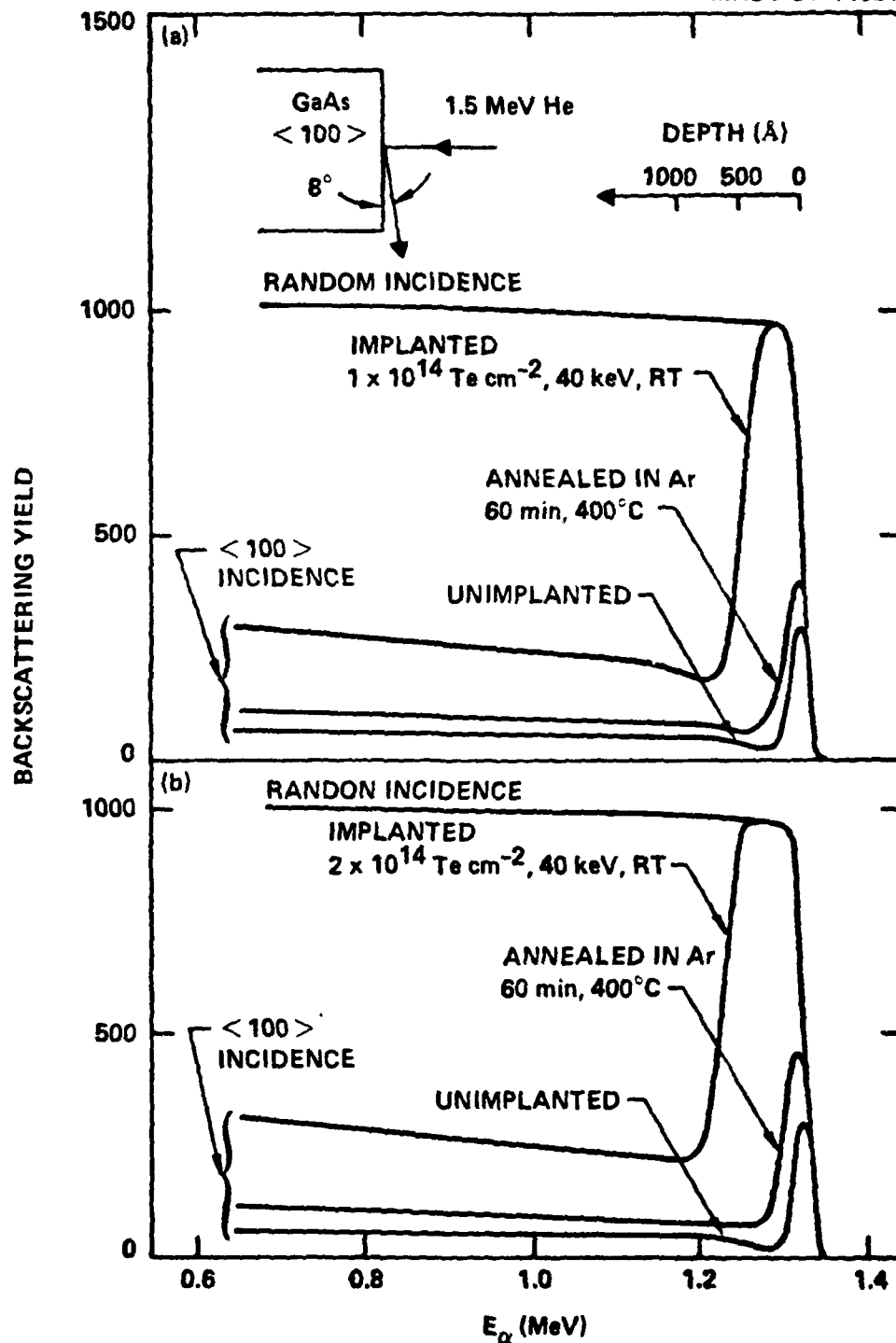
Fig. 2.2-1   Backscattering energy spectra of 1.5 MeV He+ ions at random and
<100> incidence. The sample was GaAs implanted at room tempera-
ture with 40 keV Te ions to doses of 1×10^{14} cm^{-2} (part a) and
2×10^{14} cm^{-2} (part b). Spectra are shown for the samples both
before and after annealing in flowing Ar at 400°C for 60 min.
Channeling spectra obtained with unimplanted GaAs are also shown
for comparison.

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observed previously for GaAs implanted with either donor or acceptor ions[8,9] and more recently by Kular et al.[3] The conductivity after implantation has been interpreted as a thermally assisted hopping process associated with localized states within the forbidden gap.[8] Low temperature annealing is believed to slightly order the material decreasing the number of localized states and increasing the room temperature resistivity.[3]

Table 2.2-1
Four-Point Probe Sheet Resistances
(Estimated Uncertainty ~ 10%)

Implantation Dose	R_s (MΩ/$\square$)	
	Implanted	Implanted & Annealed
1×10^{14} Te cm^{-2}	0.65	2.65
2×10^{14} Te cm^{-2}	0.50	2.50

The conclusion from this study is that although the lattice cand apparently be reordered to a near virgin state by low temperature anneal, very little electrical activity of the implanted dopant is obtained.

3.0 CIRCUIT FABRICATION AND PROCESS STABILIZATION

Processing on mask set AR6 contianing SD^{2}FL 8 × 8 multipliers was begun during this quarter. The first lot of wafers have been completed while several other lots are nearing completion. A summary of the dc parametric testing on the first lot of wafers is shown in Table 3.0-1. Most of the AR6 wafer lots are fabricated on LEC substrate material. As can be seen from the table, very satisfactory processing uniformity and reproducibility were attained. The FET threshold voltages and currents are well behaved with good uniformity as indicated by the standard deviations measured. The series resistance of the logic diode (R_s) is in a comfortable 350 to 500 Ω range indicating good ohmic contact and implantation process control. Good integrated circuit performance can be anticipated from these wafers.

Table 3.0-1
Test Device Characteristics

Wafer Number	FETs				Diodes		
	V_p (V)	σV_p (mV)	I_{dss} (mA)	σI_{dss} (%)	Rs	σR_s (%)	V_{th} (V)
11	1.041	75.7	2.887	9.7	438.7	8.4	.8089
12	1.022	83.8	2.891	12.6	482.5	10.3	.8062
13	.9322	80.5	2.782	10.3	409.8	10.6	.7888
14	1.096	115	3.370	7.4	355.3	11.3	.7949

Continuing work on reliability and second level metal process yield are discussed in the following sections.

3.1   Interconnect Yield

In order to evaluate the second level metal process, a yield test mask set has been fabricated. Details of this mask set were described in the last report.[1] Results comparing the yield of second level metal lines deposited by E-beam evaporation versus magnetron sputtering are shown in Fig. 3.1-1. The yields resulting from the magnetron sputtered wafers are much higher than the yield, from e-beam evaporated wafers. This is because the magnetron sputtered films exhibit far less metal defects (splattering) than typical evaporated films. Other factors limiting second metal yield are dust and photoresist residue. Improved wafer handling and use of a recirculated, filtered developer bath will be instituted in the near future in order to minimize the photoresist residue. In addition an improvement in the clean room environment will minimize the number of potential particles falling on the wafers as the operation is scaled up to 3 inch wafers.

Also, a new magnetron sputtering system compatible with 3 inch diameter wafers is planned in conjunction with the overall equipment upgrade directed toward large wafer processing. As mentioned in the last report, the resistivity of magnetron sputtered Au films is higher than that of e-beam evaporated films. The higher resistivity of Au films deposited by magnetron sputtering is the only
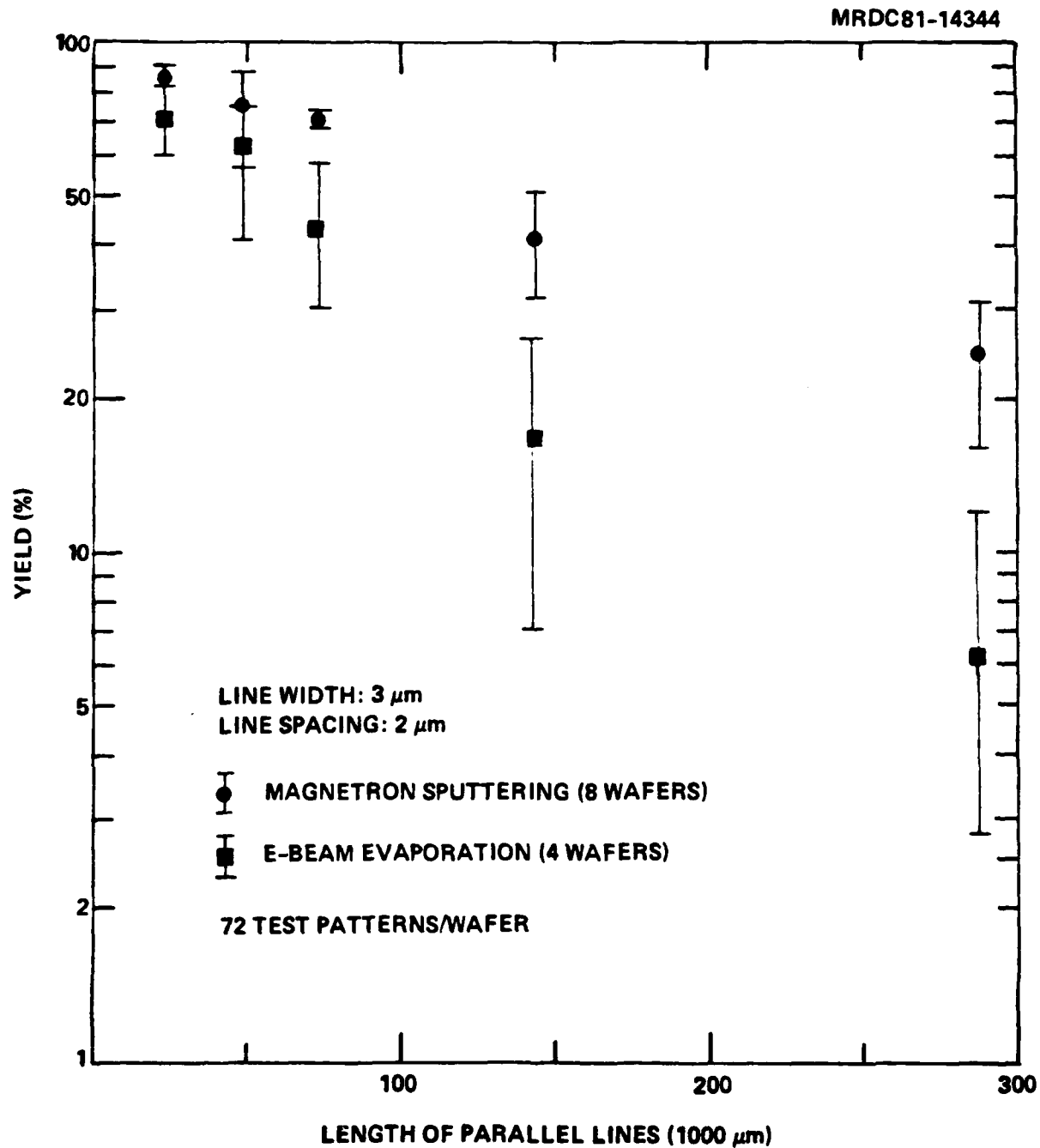
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Fig. 3.1-1   Yield of parallel second level metal lines with different metal deposition techniques.

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disadvantage of using this approach for second-level metal. However, the experimental results indicate that the resistivity of magnetron sputtered Au films can be close to that of e-beam evaporated Au film if proper sputtering conditions are used.

The test structure shown in Fig. 3.1-2 has been designed to evaluate metal line resistivities and line widths. In these experiments, the designed line widths are 1.5, 2, and 2.5 μm, and the lengths are 7930, 7930, and 6430 μm, respectively. The resistance of each line can be expressed as

$$R = \rho \frac{\ell}{A} = \rho \frac{\ell}{d(W + \Delta W)} \quad ; \tag{2}$$

where

ρ	=	resistivity
ℓ	=	line length
A	=	cross section area
d	=	thickness
W	=	designed width
ΔW	=	deviation of actual width from designed width.

Equation (2) can be rewritten as

$$\frac{\ell}{R} = \frac{d}{\rho} (W + \Delta W) \quad . \tag{3}$$

By plotting ℓ/R vs W as shown in Fig. 3.1-3, d/ρ can be determined from the slope. Knowing the metal thickness, the film resistivity, ρ, can be calculated. The difference between nominal width and real width, -ΔW, is determined from the X axis intersection. Using this technique it was found that, on the average, the ion milled second-level metal lines are 0.15 μm narrower than the designed width. This measurement technique will be used to optimize the parameters used on the new magnetron sputtering system in order to minimize the resistivity of the deposited Au interconnects.
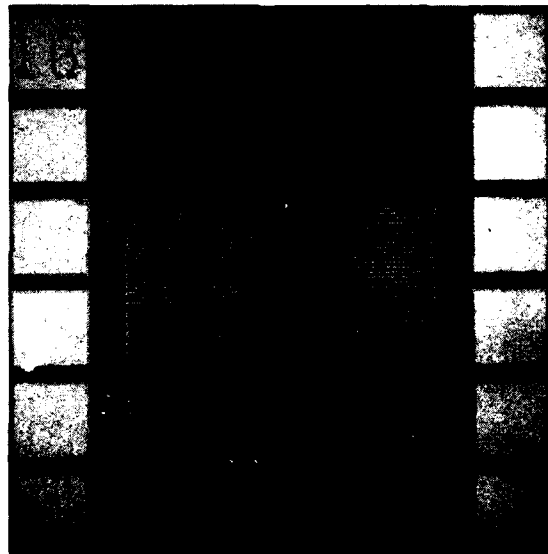
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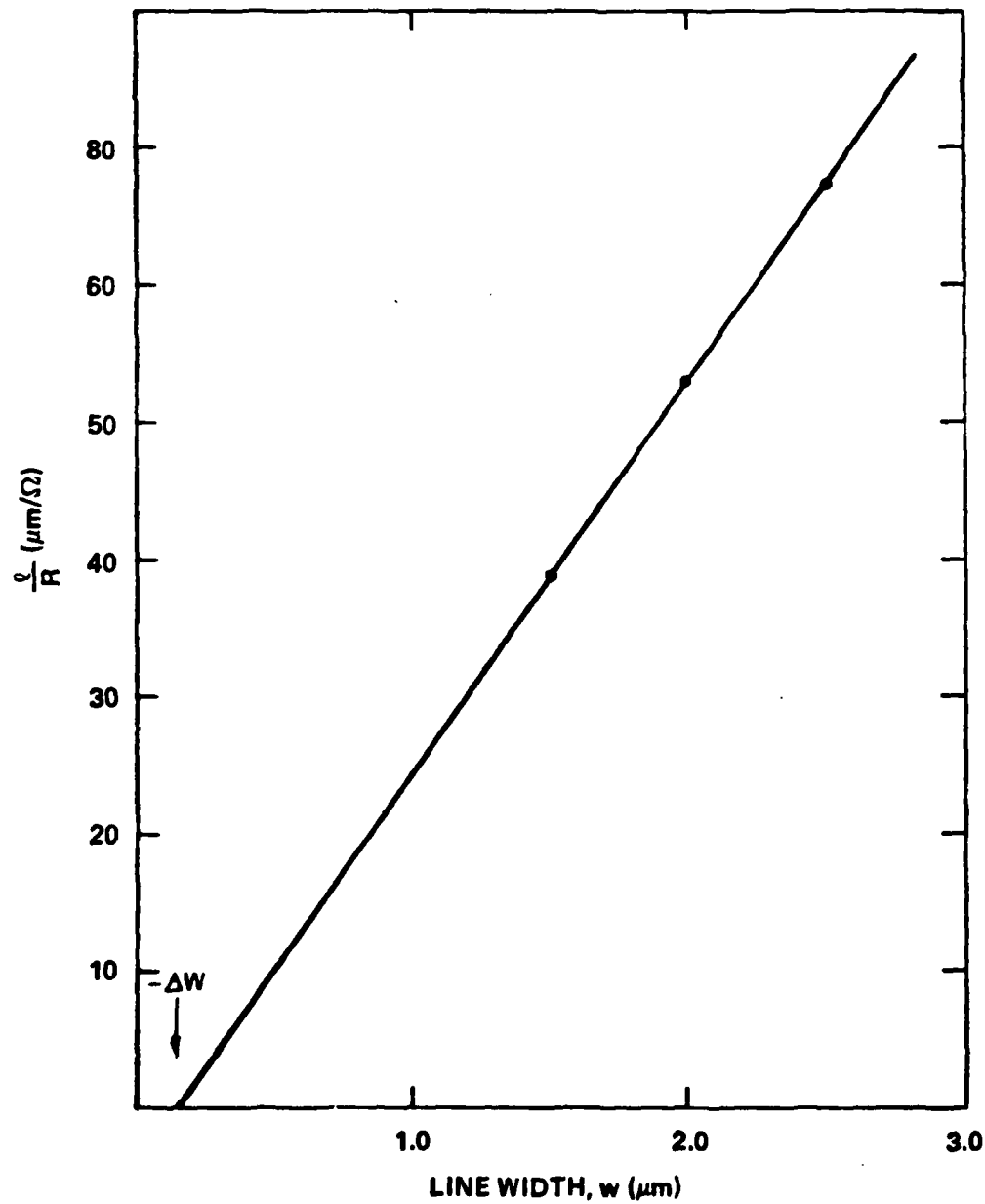Fig. 3.1-2 Metal line resistivity and line width control test structure.

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Fig. 3.1-3   Example of data from the resistivity and metal line width test
structure.

3.2   Circuit Reliability

Circuit reliability studies have been continued during the last reporting period. High temperature accelerated life tests were carried out on ohmic contacts, FETs, and ring oscillators. Initial evaluation of the activation energy associated with device degradation was carried out, and the median life of the circuits were established using the Arhenius relation. Room temperature lifetime of more than 10^{13} hours for ring oscillator circuits was predicted from the results of these tests. This data demonstrates, for the first time, that GaAs integrated circuits can be extremely reliable even though they contain many more complex structures than discrete MESFETs. Additionally, the data supports the conclusion that the current IC processes are satisfactory for the fabrication of reliable circuits.

Reliability experiments were carried out on wafers fabricated with the experiment (PX1) mask set. One wafer was cut into two halves, with one piece undergoing thermal aging at 296°C, and the other at 320°C. The ohmic contacts, FETs and the ring oscillators on each half of the wafer were mesured before and after thermal aging. In order to observe the effect of the extra doping under ohmic contacts on circuit reliability, devices with the third n^{++} implant under the ohmic contacts were also evaluated. The characteristics of the devices before and after aging are listed in Tables 3.2-1 and 3.2-2. The threshold voltage, V_p, and the saturation currents, I_{dss}, were obtained from 50 μm wide test MESFETs (1 μm gate lengths) uniformly distributed across the wafer. The contact resistance (R_c) and the specific contact resistance (r_c) were determined by the transmission line model. Nine-stage ring oscillators constructed with 10 μm wide switching FETs were measured for frequency of oscillation at fixed bias conditions.

As shown in the figures, almost no degradation was observed in ohmic contact resistance at both 296°C and 320°C. The standard ohmic contacts without the enhanced n^{++} doping are just as reliable as the contacts with the extra n^{++} implant. The threshold voltage, V_p, and the saturation current, I_{dss}, of the FETs remained stable after 22 hours at 296°C, and 9 hours at 320°C. At these times, they slowly started to degrade. The oscillating frequencies of the ring

Table 3.2-1

Characteristics of devices aged at 296°C.

*Represents devices with an n^{++} implant under the ohmic contacts.

TIME (HRS)	0	2	6.5	22	64
V_p (V)	1.169 ± 0.196	1.243 ± 0.335	1.245 ± 0.363	1.202 ± 0.341	1.176 ± 0.358
I_{DSS} (mA)	4.36 ± 0.32	4.69 ± 0.45	4.54 ± 0.43	4.38 ± 0.43	3.94 ± 0.74
V_p^* (V)	1.13 ± 0.075	1.14 ± 0.072	1.146 ± 0.062	1.1 ± 0.064	1.06 ± 0.071
I_{DSS}^* (mA)	4.57 ± 0.34	4.53 ± 0.33	4.59 ± 0.26	4.45 ± 0.31	3.9 ± 0.418
R_c (Ω)	8.59 ± 1.64	11.6 ± 2	11.7 ± 2.3	12 ± 2.5	10.71 ± 1.87
r_c (Ω-cm²)	5.33 ± 2.33 x 10⁻⁶	9.8 ± 3.7 x 10⁻⁶	1.01 ± 0.43 x 10⁻⁵	1.06 ± 0.46 x 10⁻⁵	8.25 ± 3.17 x 10⁻⁶
R_c^* (Ω)	1.99 ± 0.44	2.24 ± 0.45	2.06 ± 0.41	2.45 ± 0.53	2.36 ± 1.09
r_c^* (Ω-cm²)	2.59 ± 1.25 x 10⁻⁶	3.09 ± 1.42 x 10⁻⁶	2.45 ± 1.26 x 10⁻⁶	3.61 ± 1.9 x 10⁻⁶	4.33 ± 5.1 x 10⁻⁶
f (MHz)	763 ± 40	751 ± 31	707 ± 32	656 ± 50	578 ± 71
f* (MHz)	723 ± 50	722 ± 45	701 ± 44	642 ± 55	539 ± 78

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Table 3.2-2

Characteristics of devices aged at 320°C.
*Represents devices with an n^{++} implant under the ohmic contacts.

TIME (HRS)	0	1	3	9	25.5
V_p (V)	1.101 ± 0.049	1.123 ± 0.105	1.116 ± 0.038	1.06 ± 0.034	0.992 ± 0.038
I_{DSS} (mA)	4.09 ± 0.214	4.18 ± 0.42	4.14 ± 0.25	3.96 ± 0.165	3.5 ± 0.21
V_p^* (V)	1.103 ± 0.065	1.121 ± 0.082	1.092 ± 0.059	1.046 ± 0.047	0.965 ± 0.044
I_{DSS}^* (mA)	4.27 ± 0.41	4.07 ± 0.5	4.26 ± 0.36	3.996 ± 0.29	3.465 ± 0.393
R_c (Ω)	8.88 ± 2.03	11.42 ± 3.4	10.42 ± 2.7	11.81 ± 2.63	11.58 ± 2.5
r_c (Ω-cm²)	5.62 ± 2.92 E-6	9.72 ± 4.66 E-6	7.92 ± 3.6 E-6	1 ± 42 E-5	9.56 ± 3.68 E-6
R_c^* (Ω)	2.29 ± 0.7	2.77 ± 0.46	2.58 ± 0.48	2.73 ± 0.99	2.98 ± 0.74
r_c^* (Ω-cm²)	4.3 ± 0.27 E-6	5.25 ± 2.4 E-6	4.49 ± 2.16 E-6	5.23 ± 2.77 E-6	6.26 ± 5.1 E-6
f (MHz)	747 ± 28	693 ± 19	670 ± 17	628 ± 19	529 ± 18
f* (MHz)	713 ± 49	674 ± 55	641 ± 55	589 ± 65	464 ± 64

oscillators decreased gradually with time; degrading at a faster rate at 320°C than at 296°C. Again, there were no significant differences in the reliability of the MESFETs and ring oscillators with and without heavy ($\sim$ 40 Ω/□) doping under the ohmic contacts. These results suggest that a n region with a sheet resistance of about 400 Ω/□ and a peak carrier concentration of about 2×10^{17} cm^{-3} under the ohmic contact is sufficient to make a reliable ohmic contact.

The relation between the oscillating frequencies of thermal aged ring oscillators (without n^{++}) versus aging time is shown in Fig. 3.2-1. The frequencies were normalized with respect to the frequencies before aging. If 20% degradation in frequency is chosen as an arbitrary failure criterion for ring oscillators, the circuits would have a median life of 14 hours and 46 hours at 320°C and 296°C, respectively. Using these two numbers in the Arrhenius plot, (see Fig. 3.2-2) an activation energy of 1.42 eV is obtained. If the straight line is extrapolated to room temperature, a lifetime of more than 10^{13} hours is obtained. The activation energy obtained from these thermally aged ring oscillator circuits, is comparable to data reported on the reliability of discrete GaAs MESFETs.[11]

The results presented above demonstrates that GaAs integrated circuits containing more complicated circuit structures, and fabricated with much more complex processes than discrete MESFETs, can be made very reliable. Preliminary results on accelerated aging tests for devices under bias are underway. Results should be available for the next quarterly report.
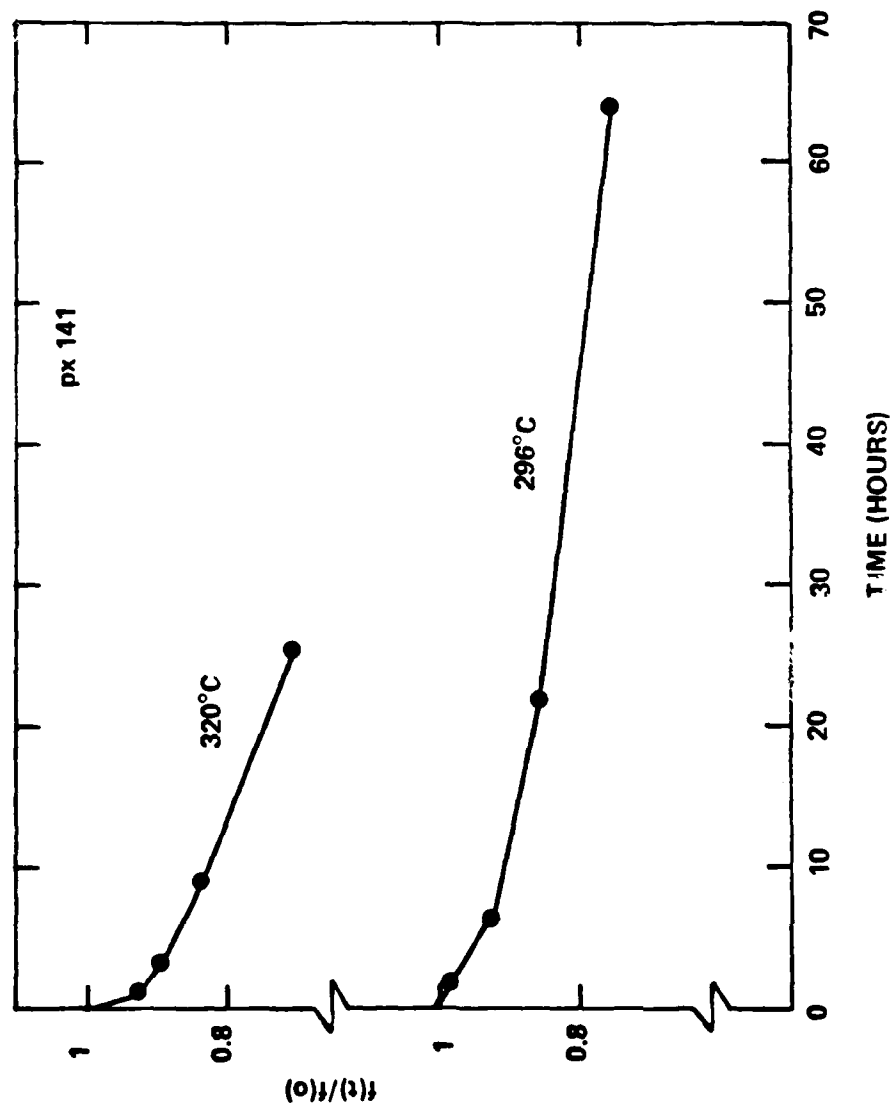
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Fig. 3.2-1 Thermal aging effects on the frequency of oscillation of SDFL ring oscillators.
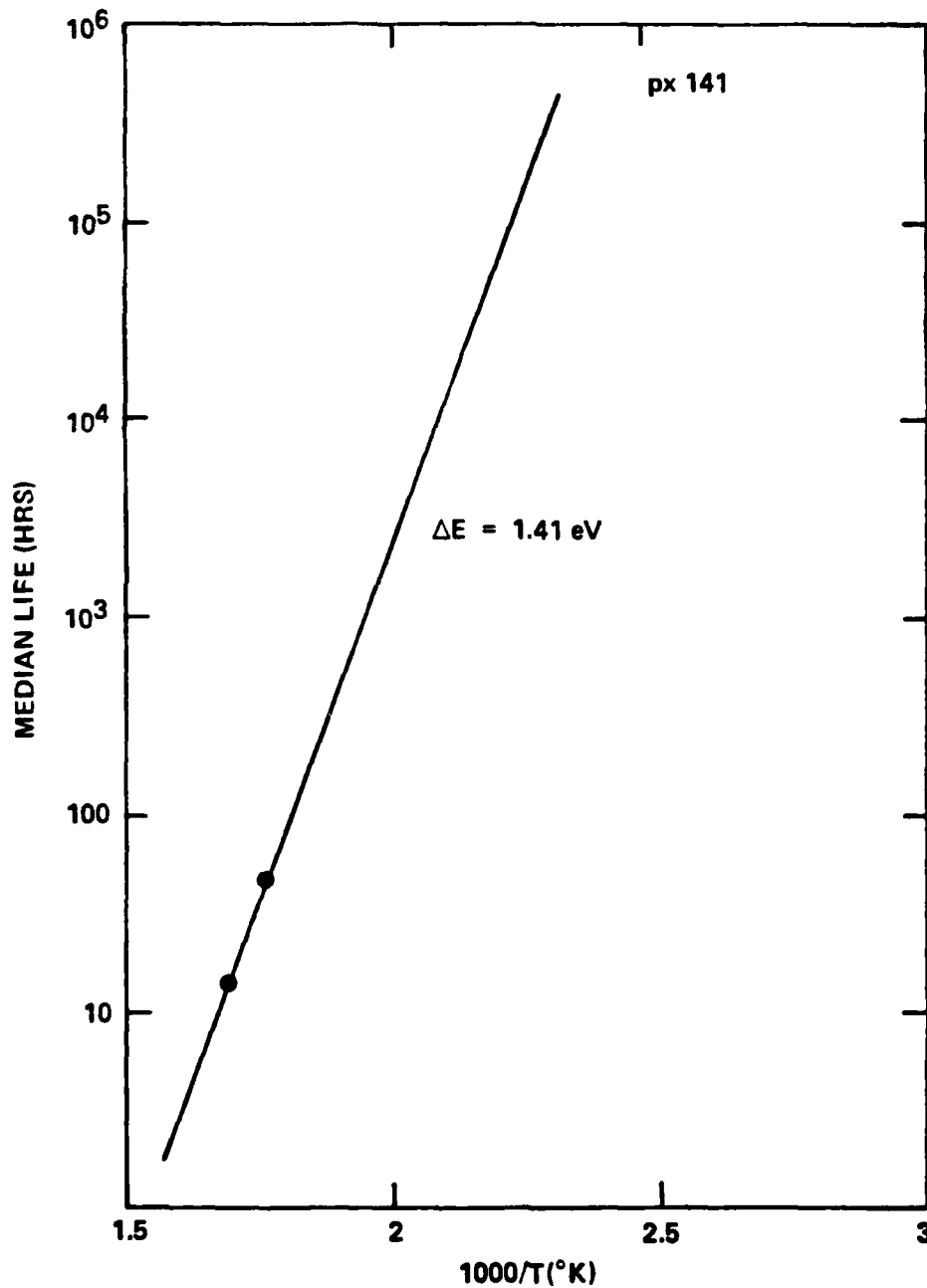
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Fig. 3.2-2   Arrhenius plot for GaAs ring oscillators thermally aged at 296°C and 320°C with a 210% decrease in frequency of oscillation used as a failure criteria.

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4.0 DEVICE MODELING

Three modeling tasks are carried out at North Carolina State University.

4.1 Two-Dimensional Numerical Modeling of FET Devices

The two-dimensional modeling has progressed considerably since the last reporting period. The device structure being considered is a basic ion-implanted channel FET with a 1 µm gate and spacings of 0.5 µm between source and gate and between drain and gate. The work during this period has concentrated on:

a. Modeling FETs with an ion-implanted profile as opposed to uniformly doped FETs.

b. Developing techniques for calculating the small-signal parameters of the FETs.

Data for the ion-implanted channel has been taken from curves of experimental devices. The assumed profile peaks at 1-$2 \times 10^{17}/cm^3$ at around 0.1 µm and decreases to around $10^{15}/cm^3$ at 0.3 µm and to about $10^{13}/cm^3$ at 0.5 µm.

One complete set of calculations is shown in Figs. 4.1-1 to 4.1-6. The I_d vs V_d characteristic is shown in Fig. 1d for gate voltages from 0.5 to -0.5 V, assuming a Schottky barrier height of 0.8 V. The general features of the calculations are in good agreement with experimental devices, i.e., a saturation voltage of around 1.0 V and a pinch-off voltage of around 0.5 V. The exact spacings between the curves for constant V_{gs} depend somewhat on the shape of the implantation profile assumed for the calculation.

The major discrepancy between the calculations and experimental data appears to be a larger drain conductance in the saturation region observed in the calculations when compared with the experimental devices. This will be considered again later in this report.
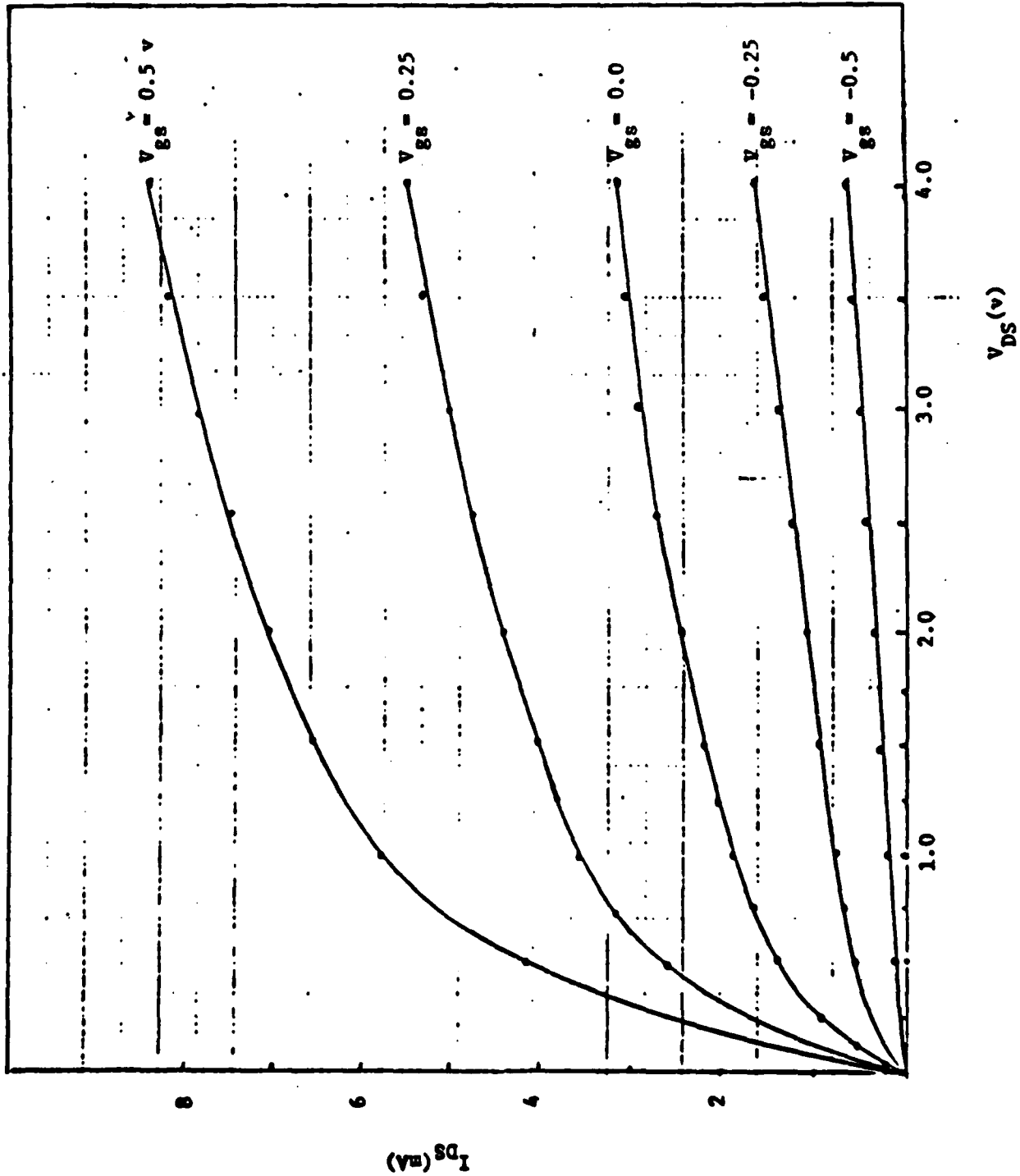
MRDC41070.12QR

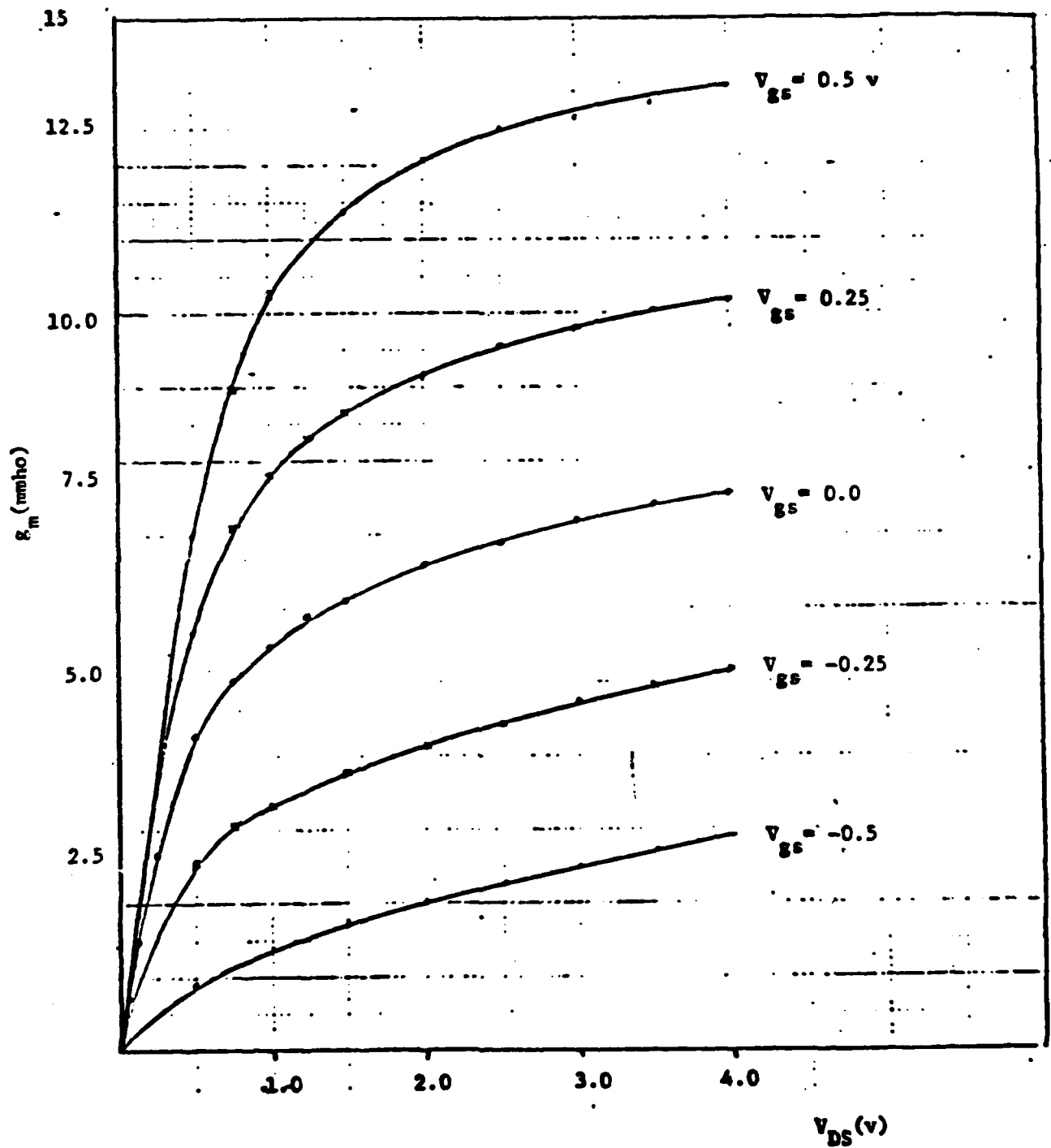Fig. 4.1-1 Drain current as a function of drain voltage.

Fig. 4.1-2   Transconductance as a function of drain voltage.
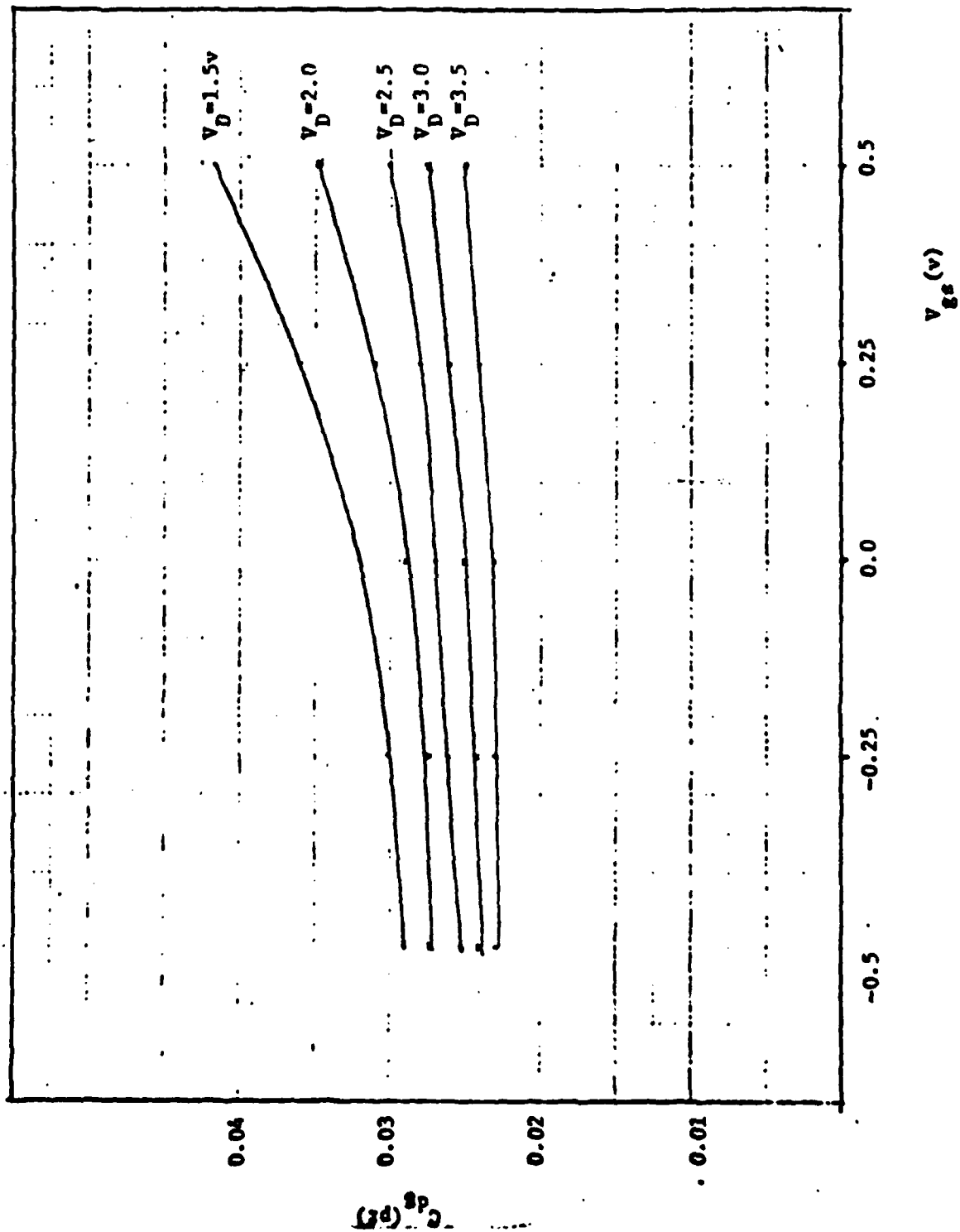
Fig. 4.1-3   Drain-to-gate capacitance as a function of gate voltage.
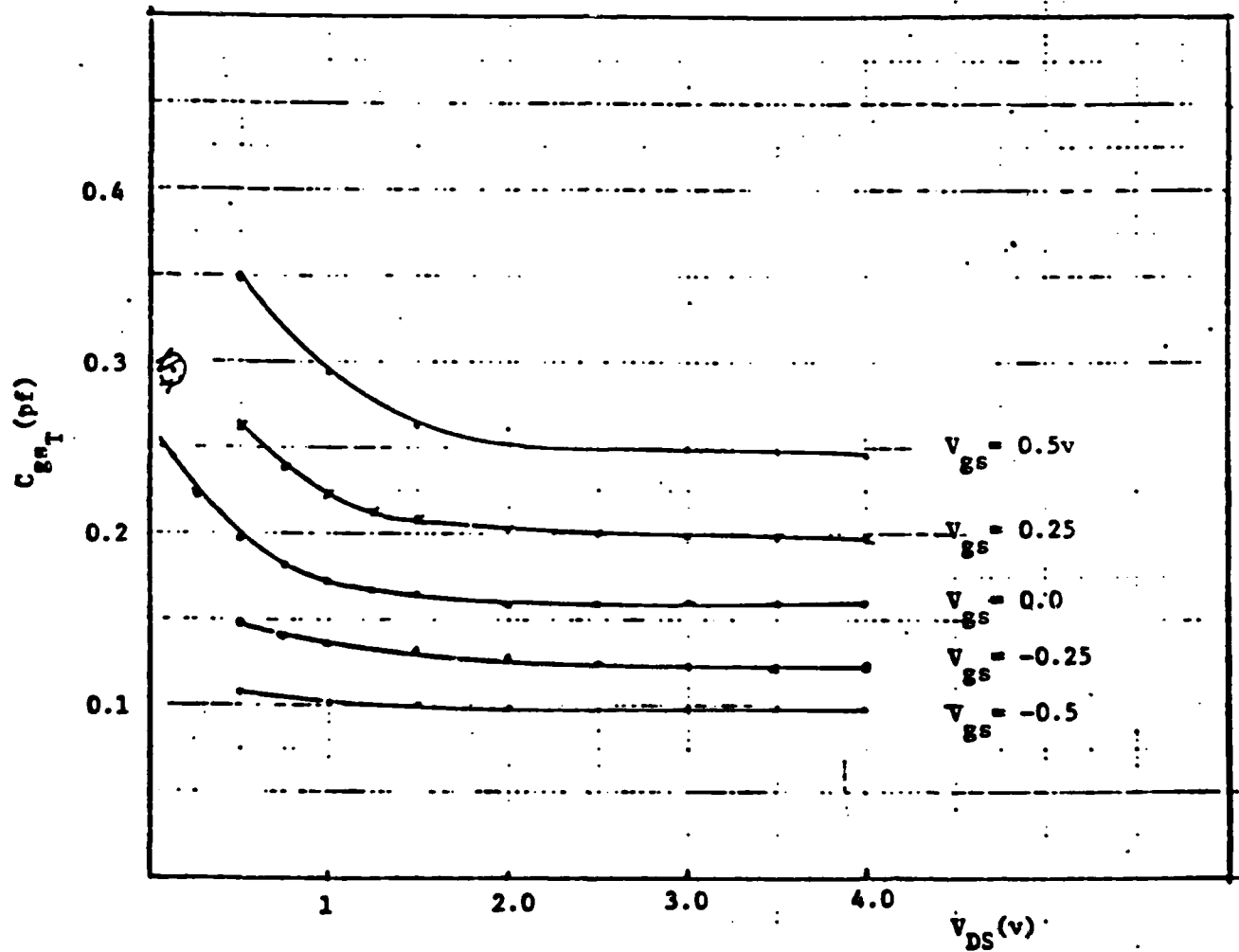
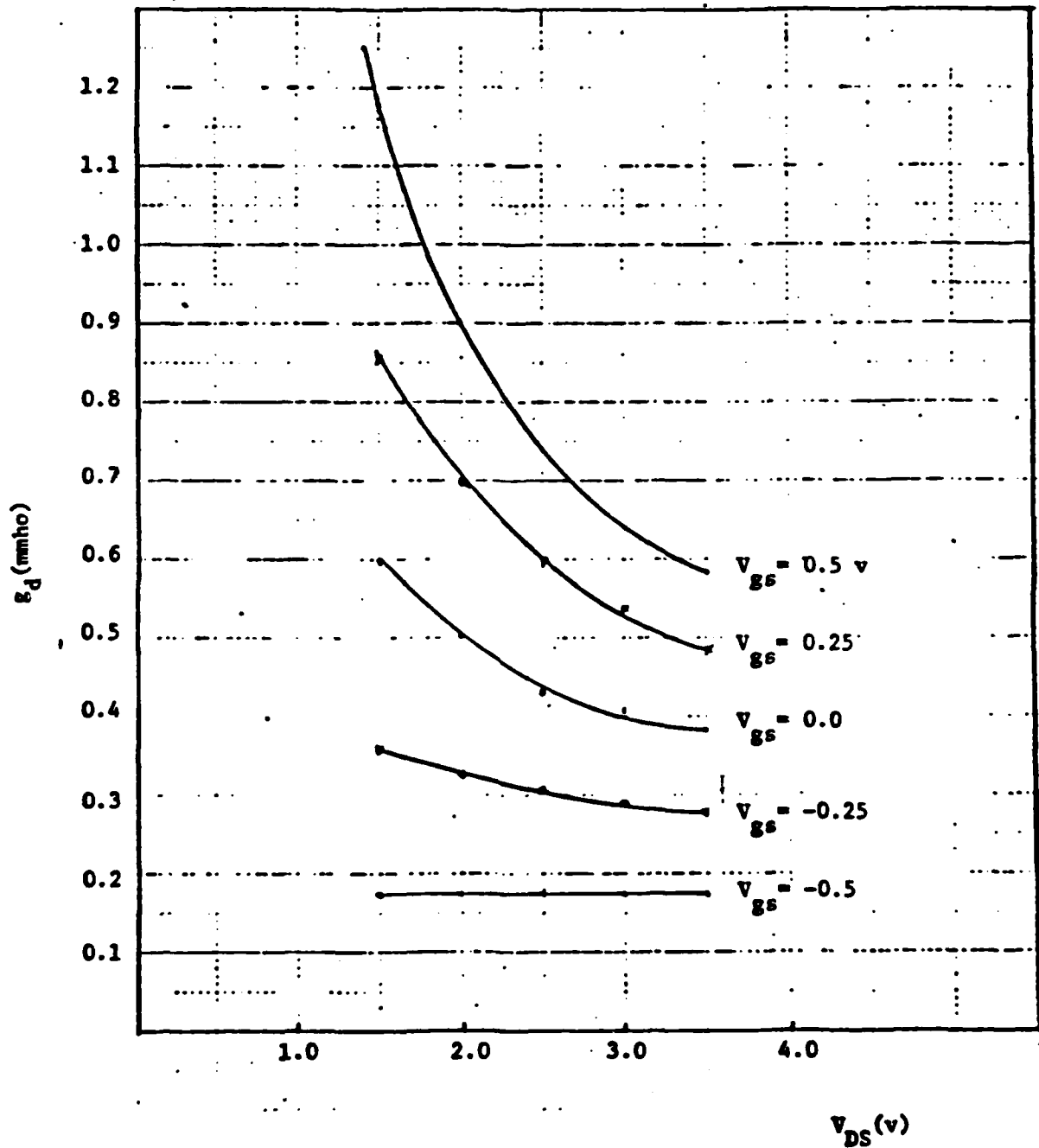Fig. 4.1-4   Gate-to-source capacitance as a function of drain voltage.

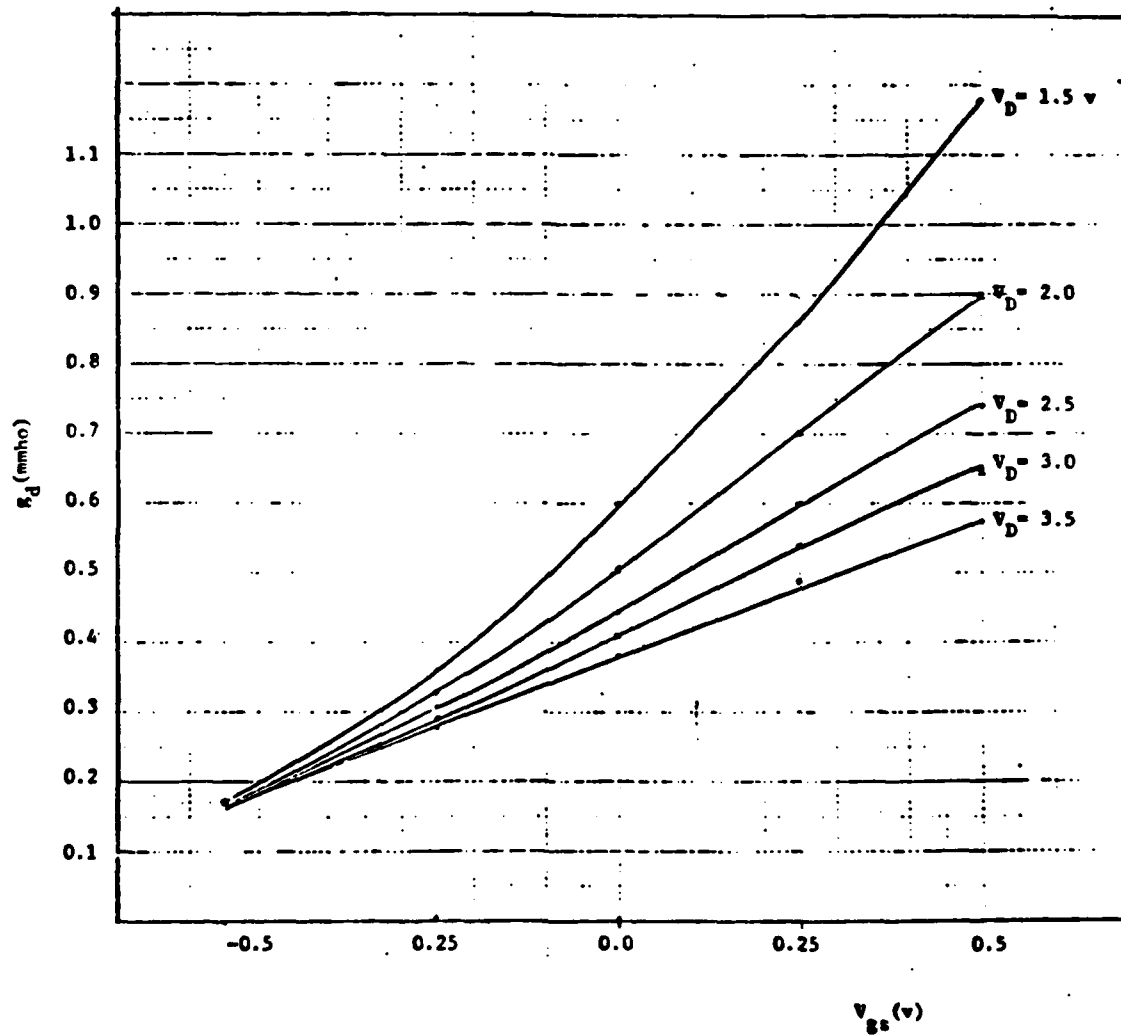Fig. 4.1-5   Drain conductance as a function of drain voltage.

Fig. 4.1-6   Drain conductance as a function of gate voltage

In order to test the calculations of small-signal parameters, a series of calculations were made, and the results are shown in Figs. 4.1-2 to 4.1-6. The numerical techniques for evaluating g_m, C_{gs}, C_{gd}, and g_d appear to be working satisfactorily, and the results in general are what are to be expected as functions of bias voltages. The gate-to-source capacitance values are in the range of 5 to 10 times the gate-to-drain capacitance values. Also, it can be noted that the transconductance increases approximately linearly with gate voltage in the saturation region.

A brief discussion of the output conductance is in order since the value of g_d in the saturation region in Fig. 4.1-1 is larger than that of experimental devices. First it should be noted that the FET modeled in Fig. 4.1-1 was assumed to have uniformly, heavily-doped source and drain regions extending to a depth of 0.5 μm. After observing the large output conductance, calculations have recently been made for devices with ion-implanted source and drain regions and the initial results indicate that the output conductance drops significantly for the case of the ion-implanted contacts. Such a large effect due to the nature of the contact regions was unexpected. However, some understanding of the physics behind this phenomena is beginning to emerge, and this effect will be discussed in detail in future reports.

4.2   Analytical Modeling of MESFET Devices

Two analytic MESFET models are under development. One model is similar to that reported by Yamaguchi and Kodera. In this approach, modeling of the source-gate and drain-gate capacitances is under way. A non-abrupt pn junction model has been adopted for the MESFET. In the region beneath the gate, the charge is obtained through a solution of Poisson's equation. This analysis shows that an effective depletion width which is larger by one-half the thickness of the transition region is obtained. Therefore, the non-abrupt model results in a significant reduction in the source- and drain-gate capacitances.

Edge effect capacitances have been studied by two methods. The results are not consistent, and further work is necessary to obtain a final result.

The second model employs a technique similar to that reported by Pucel. This model has been used to obtain values for equivalent circuit elements that are in good agreement with experimentally obtained values for flat profile FETs. Currently the model is being modified to handle ion-implanted profiles through use of a Fourier series representation of the doping concentration. This approach looks promising and preliminary results are encouraging. A technique to obtain a potential dependent gate-drain capacitance has been developed. Preliminary results are in good agreement with values obtained from thetwo-dimensional model.

An analytic expression that describes the carrier mobility and velocity as a function of doping has been derived. This expression was determined from Monte Carlo transport data by a curve fitting technique. The expression has the form

$$\mu(N_d) = \frac{1}{1 + \left(\frac{\log N_d}{K}\right)^n} \tag{3}$$

where k and n are empirically determined constants. This expression is being used in both the two-dimensional and analytic models to describe carrier transport as a function of depth in the ion-implanted devices.

4.3   Monte Carlo Analysis

In this work, a two-dimensional device analysis program is used to calculate an initial guess for the electric field $E_0(x,y)$ in a device. Subsequently, a two-dimensional Monte Carlo program and a program for solving Poisson's equation are used (iteratively) to obtain self-consistent profiles for the field $E(x,y)$ and the charge $\rho(x,y)$.

Results from the first trial run (one iteration) are shown in Figs. 4.3-1 and 4.3-2. Figure 4.3-1 shows the net charge distribution obtained from the two-dimensional device analysis program. Figure 4.3-2 shows the net charge distribution obtained from the two-dimensional Monte Carlo program for 250,000
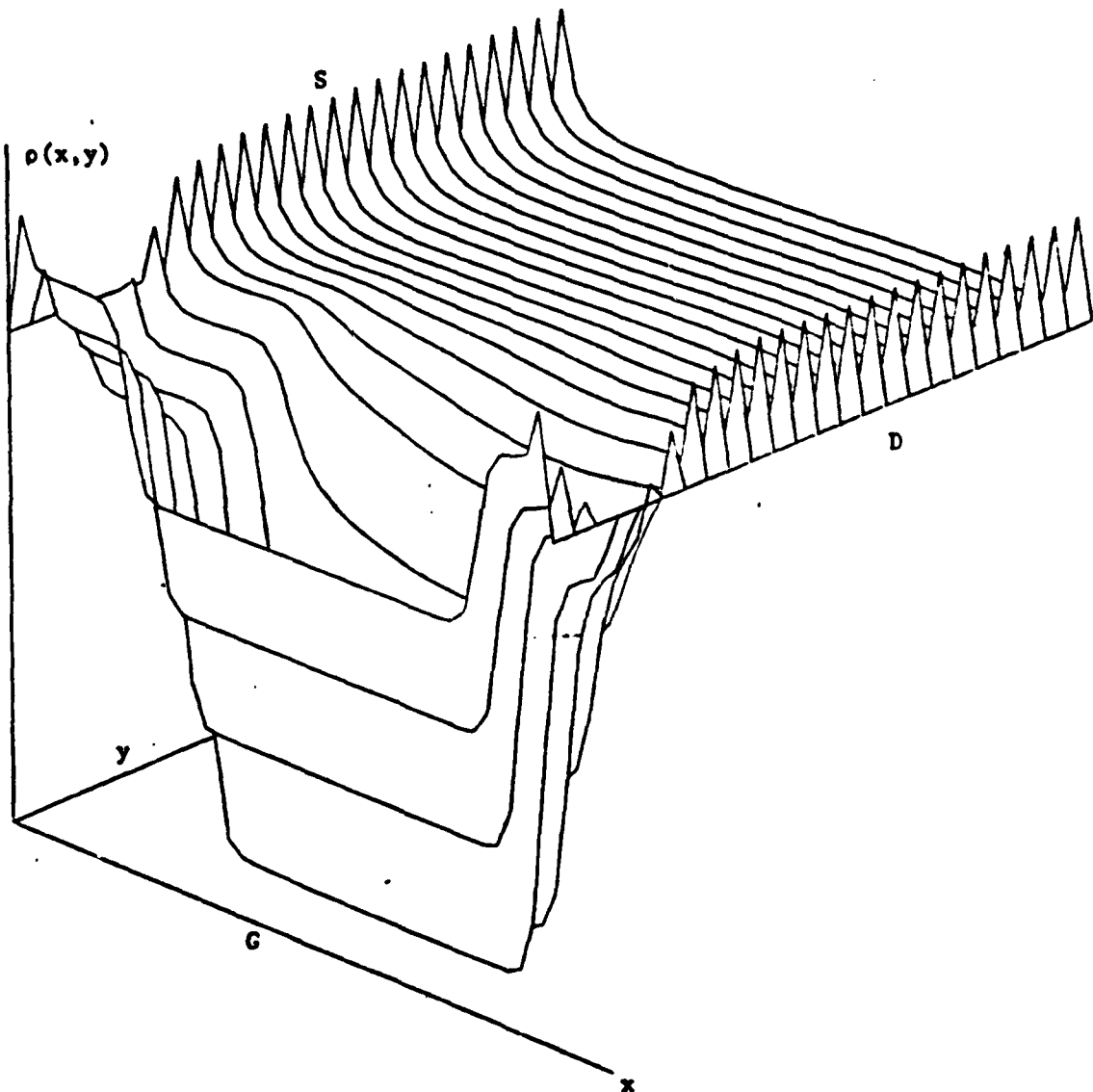
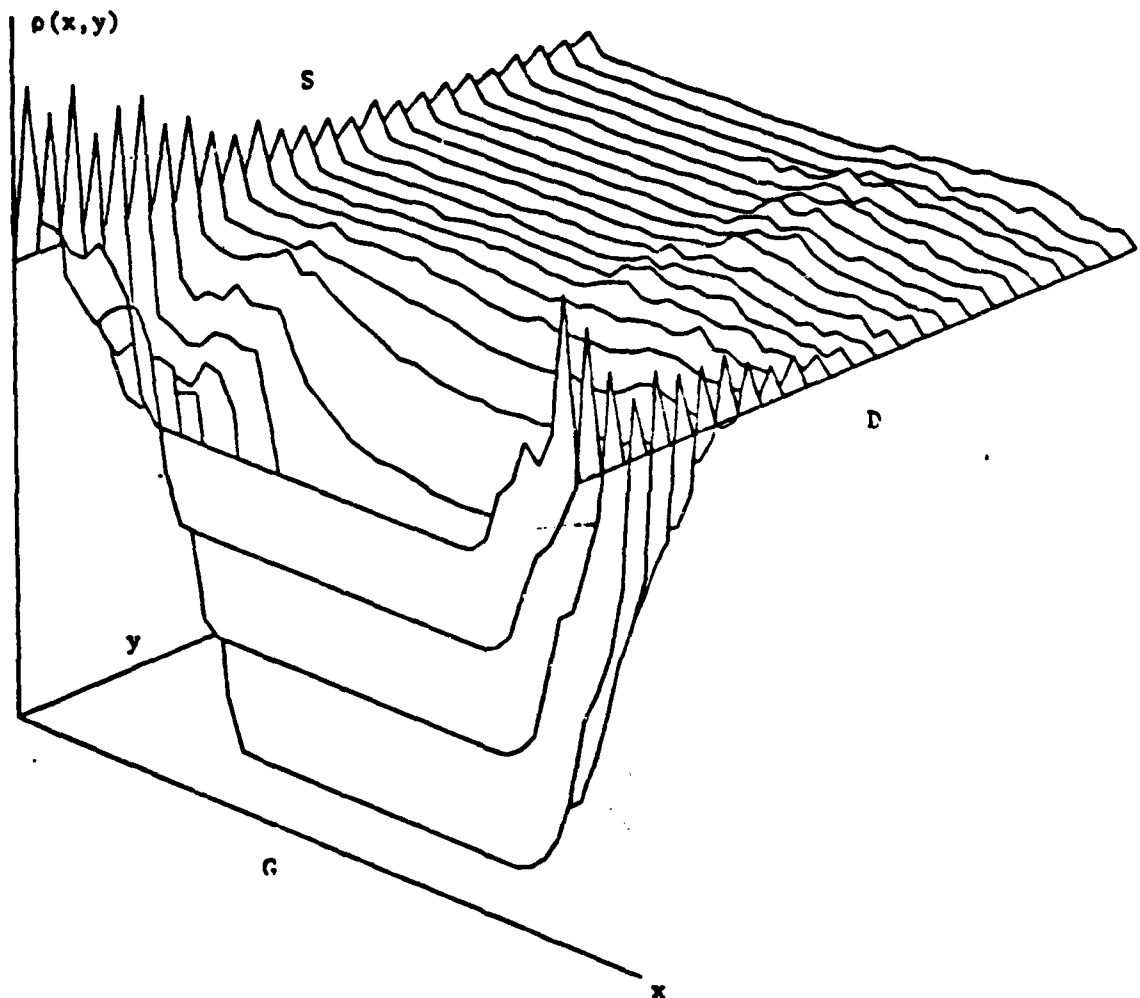Fig. 4.3-1   Net charge density obtained from device analysis program.

Fig. 4.3-2   Net charge density obtained from the Monte Carlo simulation.

scattering events (approximately 2500 carriers). The structure of the device is that described in Section 4.1 of this report, with $V_{GS} = 0$ and $V_{DS} = 2.5$ V.

There is some scatter in the Monte Carlo data, as expected, but on the whole the distributions of Figs. 4.3-1 and 4.3-2 are very similar. There is one difference tha may be significant: the Monte Carlo results show some accumulation at about two-thirds of the distance from the source to the drain (Fig. 4.3-2). This accumulation is not present in the charge distribution obtained from the device analysis program (Fig. 4.3-1). There is some reason to believe that this accumulation is real, because it occurs in a region where the fields are quite high. It may be that the device analysis does not show this effect because it uses a static model for the velocity-field characteristic. The Monte Carlo analysis, on the other hand, uses a dynamic model which correctly describes the instantaneous velocity-field relation.

The results shown in Fig. 4.3-2 are quite encouraging. They show that the Monte Carlo method is a promising alternative to standard device analysis methods, especially for small (submicron) devices, where standard models may give wrong results.

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